AMENDMENTS TO THE CLAIMS:

Please amend claims 4 and 14 as follows below. This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims

1. (Previously Presented) A semiconductor integrated circuit comprising:

a central processing unit;

a main memory control unit for controlling a main memory;

an I/O channel control unit for controlling a peripheral device;

a first bus for connecting the central processing unit, main memory control unit and I/O channel control unit to each other;

a local memory for storing information;

a second bus for connecting the local memory to the central processing unit;

an access control means for accessing the local memory in response to a request from outside; and

a third bus for directly connecting the local memory to the access control means.

2. (Original) The semiconductor integrated circuit according to claim 1, wherein the local memory includes a first access port connected to the second bus and a second access port connected to the third bus.

3. (Original) The semiconductor integrated circuit according to claim 2, wherein the local memory is a dual-port RAM having the first and second access ports.

4. (Currently Amended) A semiconductor integrated circuit comprising:

a central processing unit;

a main memory control unit for controlling a main memory;

an I/O channel control unit for controlling a peripheral device;

a first bus for connecting the central processing unit, main memory control unit and I/O channel control unit to each other;

a local memory for storing information;

a second bus for connecting the local memory to the central processing unit;

an access control means for accessing the local memory in response to a request from outside;

a third bus for connecting the local memory to the access control means; and

~~The semiconductor integrated circuit according to claim 1, further comprising~~ selection means connected between the second and third buses and the local memory for selecting the second bus or the third bus so as to connect the selected bus to the local memory.

5. (Original) The semiconductor integrated circuit according to claim 4, further comprising arbitration means for issuing an instruction to the selection means regarding selection of the second or third bus, on the basis of a request to access the local memory from the central processing unit and a request to access the local memory from the access control means.

6. (Original) The semiconductor integrated circuit according to claim 5, wherein the arbitration means prioritizes the access request from the central processing unit over the access request from the access control means.

7. (Original) The semiconductor integrated circuit according to claim 2, wherein the local memory is RAM with an access port on one side.

8. (Original) The semiconductor integrated circuit according to claim 5, wherein the arbitration means prioritizes the access request from the access control means over the access request from the central processing unit.

9. (Original) The semiconductor integrated circuit according to claim 1, wherein the local memory has a smaller capacity than the main memory but has a higher access speed than the main memory.

10. (Original) The semiconductor integrated circuit according to claim 5, wherein the arbitration means generates and issues a selection result signal, which indicates the selected bus, to the outside.

11. (Previously Presented) A semiconductor integrated circuit comprising:

a central processing unit;

a main memory controller for controlling a main memory;

an I/O channel controller for controlling a peripheral device;

a first bus for connecting the central processing unit, main memory controller and I/O channel controller to each other;

a local memory for storing information;

a second bus for connecting the local memory to the central processing unit;

an access controller for accessing the local memory in response to a request from outside; and

a third bus for directly connecting the local memory to the access controller.

12. (Original) The semiconductor integrated circuit according to claim 11, wherein the local memory includes a first access port connected to the second bus and a second access port connected to the third bus.

13. (Original) The semiconductor integrated circuit according to claim 12, wherein the local memory is a dual-port RAM having the first and second access ports.

14. (Currently Amended) A semiconductor integrated circuit comprising:

a central processing unit;

a main memory controller for controlling a main memory;

an I/O channel controller for controlling a peripheral device;

a first bus for connecting the central processing unit, main memory controller and I/O channel controller to each other;

a local memory for storing information;

a second bus for connecting the local memory to the central processing unit;

an access controller for accessing the local memory in response to a request from outside;

a third bus for connecting the local memory to the access controller; and

~~The semiconductor integrated circuit according to claim 11, further comprising~~ a selector connected between the second and third buses and the local memory for selecting the second bus or the third bus so as to connect the selected bus to the local memory.

15. (Original) The semiconductor integrated circuit according to claim 14, further comprising an arbitration circuit for issuing an instruction to the selector regarding selection of the second or third bus, on the basis of an access request to the local memory from the central processing unit and an access request to the local memory from the access controller.

16. (Previously Presented) The semiconductor integrated circuit according to claim 15, wherein the arbitration circuit prioritizes the access request from the central processing unit over the access request from the access controller.

17. (Original) The semiconductor integrated circuit according to claim 12, wherein the local memory is RAM with an access port on one side.

18. (Original) The semiconductor integrated circuit according to claim 15, wherein the arbitration circuit prioritizes the access request from the access controller over the access request from the central processing unit.

19. (Original) The semiconductor integrated circuit according to claim 11, wherein the local memory has a smaller capacity than the main memory but has a higher access speed than the main memory.

20. (Original) The semiconductor integrated circuit according to claim 15, wherein the arbitration means generates and issues a selection result signal, which indicates the selected bus, to the outside.